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06EC63

Sixth Semester B.E. Degree Examination, June/July 2015
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the working of S/H circuit and track and hold circuit. **(08 Marks)**

b. State and explain specification of DAC. **(12 Marks)**

2 a. How to lower the output capacitance using binary switches? Explain with diagram. **(06 Marks)**

b. With neat circuit, diagram explain R-2R ladder network for DAC. **(06 Marks)**

c. Design 3 bit DAC using R-2R architecture with R = 1 KΩ, R_F = 2KΩ and V_{REF} = 5V. Assume the resistance of the switches negligible. Determine the value of i_{TOT} for each digital input and the corresponding output voltage. **(08 Marks)**

3 a. With the help of neat circuit diagram, explain the working of flash ADC. **(08 Marks)**

b. Design 3-bit flash converter, listing the values of the voltage at each resistor tap, and draw the transfer curve for V_{IN} = 0 to 5V. Assume V_{REF} = 5V. Construct a table listing the values of the thermometer code and the output of the decoder for V_{IN} = 1.5V, 3.0V, 4.5V. **(12 Marks)**

4 a. Analog multipliers find extensive use in communication systems. Prove with voltage characteristic of a four quadrant multiplier. **(08 Marks)**

b. Draw the CMOS analog multiplier circuit. Briefly explain the biasing of the multiplying quad. **(12 Marks)**

PART – B

5 a. With the help of block diagram, explain decimation for ADCs interpolating filters for DACs. **(10 Marks)**

b. Implement a sinc band pas filter. **(05 Marks)**

c. Explain the term frequency sampling filters. **(05 Marks)**

6 a. With neat sketch, describe CMOS process flow. **(10 Marks)**

b. Draw and explain CV curve, layout and cross sectional view for natural MOSFET capacitor. Also briefly describe floating MOS capacitor. **(10 Marks)**

7 a. Implement delay element using:
i) Pass transistors and CMOS inverters.
ii) Clocked CMOS logic.
iii) TSPC. **(12 Marks)**

b. Briefly explain four bit pipelined adder with delay elements. Implement full adder using dynamic logic. **(08 Marks)**

8 a. Explain the following terms related with analog circuit design:
   i) Selecting channel length.
   ii) Small signal transconductance.
   iii) MOSFET transition frequency. **(12 Marks)**

   b. For the given A.C. small signal circuit shown in Fig.Q.8(b), determine the small signal resistance seen by the test voltage V_{test}. **(08 Marks)**

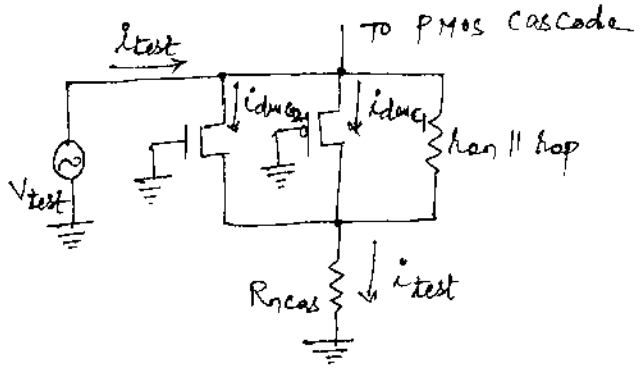

Fig.Q.8(b)

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